HYBRID PLANAR AND FinFET CMOS DEVICES

Abstract

The present invention provides an integrated semiconductor circuit containing a planar single gated FET and a FinFET located on the same SOI substrate. Specifically, the integrated semiconductor circuit includes a FinFET and a planar single gated FET located atop a buried insulating layer of an silicon-on-insulator substrate, the planar single gated FET is located on a surface of a patterned top semiconductor layer of the silicon-on-insulator substrate and the FinFET has a vertical channel that is perpendicular to the planar single gated FET. A method of forming a method such an integrated circuit is also provided. In the method, resist imaging and a patterned hard mask are used in trimming the width of the FinFET active device region and subsequent resist imaging and etching are used in thinning the thickness of the FET device area. The trimmed active FinFET device region is formed such that it lies perpendicular to the thinned planar single gated FET device region.